

What is claimed is:

1 1. A stacked gate flash memory cell having two
2 symmetrical memory structures therein, comprising:
3 a substrate having a trench therein;
4 a conductive layer disposed on the bottom of the
5 trench;
6 a pair of source regions, each disposed in the
7 substrate adjacent to one sidewall of the
8 trench, electrically connecting the conductive
9 layer;
10 a source isolation layer disposed on the conductive
11 layer;
12 a pair of tunnel oxide layers, respectively disposed
13 on one sidewall of the trench, contacting the
14 source regions thereby;
15 a pair of floating gates, respectively disposed on
16 the source isolation layer, contacting the
17 tunnel oxide layers thereby;
18 a pair of inter-gate dielectric layers, respectively
19 overlying the floating gate thereby;
20 a pair of control gates, respectively overlying the
21 inter-gate dielectric layer thereby;
22 an insulating layer disposed in the trench,
23 isolating the two control gates, forming two
24 symmetrical memory structures therein; and
25 a drain region disposed in the substrate adjacent to
26 the trench.

1 2. The flash memory cell as claimed in claim 1,
2 wherein the substrate is P-type silicon substrate.

1 3. The flash memory cell as claimed in claim 1,
2 wherein a bottom insulating layer is further disposed
3 under the conductive layer.

1 4. The flash memory cell as claimed in claim 3,
2 wherein the bottom insulating layer is silicon dioxide.

1 5. The flash memory cell as claimed in claim 1,
2 wherein the conductive layer is N-type dopant doped
3 polysilicon.

1 6. The flash memory cell as claimed in claim 1,
2 wherein the source isolation layer is silicon dioxide.

1 7. The flash memory cell as claimed in claim 1,
2 wherein the tunnel oxide layer is silicon dioxide.

1 8. The flash memory cell as claimed in claim 1,
2 wherein the floating gate is N-type dopant doped
3 polysilicon.

1 9. The flash memory cell as claimed in claim 1,
2 wherein the floating gate is a composite polysilicon
3 layer composed of a second polysilicon layer and a third
4 polysilicon layer.

1 10. The flash memory cell as claimed in claim 1,
2 wherein the floating gate is L-shaped or reverse L-shaped
3 (J).

1 11. The flash memory cell as claimed in claim 1,
2 wherein the inter-gate dielectric layer is silicon
3 dioxide.

1 12. The flash memory cell as claimed in claim 1,
2 wherein the control gate is N-type dopant doped
3 polysilicon.

1 13. The flash memory cell as claimed in claim 1,
2 wherein the conductive layer is composed of a polysilicon
3 layer adjacent to sidewalls of the trench and a source
4 line material layer in the trench.

1 14. A method of fabricating stacked gate flash
2 memory cells, comprising the steps of:

3 providing a substrate;

4 forming a plurality of parallel long trenches along
5 a first direction in the substrate;

6 forming a conductive layer and a pair of source
7 regions on the bottom of each long trench,
8 wherein the source regions are respectively
9 disposed in the substrate adjacent to two
10 sidewalls of each long trench and electrically
11 connected to the conductive layer;

12 forming a source isolation layer on each conductive
13 layer;

14 forming a tunnel oxide layer on two sidewalls of
15 each long trench, contacting the source region
16 thereby;

forming a pair of floating gates on the source isolation layer, respectively contacting the tunnel oxide layer;
forming a pair of inter-gate dielectric layers, respectively overlying the floating gate;
forming a pair of control gates, respectively overlying the inter-gate dielectric layer;
forming a second insulating layer in each long trench, isolating the control gates;
forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches; and
forming a drain region in the substrate adjacent to each cell trench.

15. The method as claimed in claim 14, wherein the first direction is perpendicular to the second direction.

16. The method as claimed in claim 14, wherein the substrate is P-type silicon substrate.

17. The method as claimed in claim 14, further comprising, before forming a plurality of parallel long trenches along a first direction in the substrate, the step of sequentially forming a pad oxide layer and a mask layer on the substrate.

18. The method as claimed in claim 17, wherein the mask layer is silicon nitride.

1 19. The method as claimed in claim 14, wherein the
2 source isolation layer is sequentially formed by LPCVD
3 and HDPCVD.

1 20. The method as claimed in claim 14, further
2 comprising, before forming a conductive layer and a pair
3 of source regions on the bottom of each long trench, the
4 step of forming a bottom insulating layer in the bottom
5 of each long trench.

1 21. The method as claimed in claim 14, wherein
2 forming a conductive layer and a pair of source regions
3 on the bottom of each long trench further comprises the
4 steps of:

5 forming a source line material layer in each long
6 trench, exposing portions of the bottom
7 insulating layer therein;

8 removing the exposed bottom insulating layer,
9 partially exposing the sidewalls of each long
10 trench;

11 forming a first spacer on the sidewalls of each long
12 trench;

13 etching the source line material layer, exposing
14 portions of the bottom insulating layer
15 adjacent to sidewalls of each long trench;

16 removing the exposed bottom insulating layer,
17 respectively forming a first sidewall gap on
18 the sidewalls of each long trench;

19 conformally depositing a polysilicon layer in each
20 long trench, filling the first sidewall gaps;

21 performing a thermal annealing process, forming a
22 pair of source regions in the substrate
23 adjacent to two sidewalls of each long trench;
24 and
25 etching the polysilicon layer, leaving portions of
26 the polysilicon layer in the first sidewall
27 gaps adjacent to the source line material
28 layer, forming a conductive layer composed of
29 the source material layer and the adjacent
30 polysilicon layers in each long trench, wherein
31 the source regions are electrically connected
32 with the conductive layer.

1 22. The method as claimed in claim 21, wherein the
2 method for depositing the source line material layer is
3 chemical vapor deposition (CVD).

1 23. The method as claimed in claim 21, wherein the
2 method for removing the exposed bottom insulating layer
3 is wet etching.

1 24. The method as claimed in claim 14, further
2 comprising, before forming a tunnel oxide layer on two
3 sidewalls of each long trench, the step of performing a
4 threshold voltage implantation on the sidewalls of each
5 long trench.

1 25. The method as claimed in claim 14, wherein
2 forming a pair of floating gates on the source isolation
3 layer, and thereby respectively contacting the tunnel
4 oxide layer further comprises the steps of:

5 conformally depositing a second polysilicon layer in
6 each long trench, contacting the tunnel oxide
7 layers therein;
8 forming a protective layer in each long trench,
9 exposing portions of the second polysilicon
10 layer;
11 removing portions of the second polysilicon layer
12 exposed by the protective layer, forming a U-
13 shaped second polysilicon layer therein;
14 forming a pair of second spacers, respectively
15 disposed on the vertical portions of the U-
16 shaped second polysilicon layer;
17 removing the protecting layer;
18 conformally depositing a third polysilicon layer in
19 each long trench; and
20 etching the third polysilicon layer and the U-shaped
21 second polysilicon layer until the source
22 isolation layer is exposed, leaving a composite
23 polysilicon layer composed of the second
24 polysilicon layer and the third polysilicon
25 layer on the two sides of the long trench as a
26 floating gate, wherein the floating gate is L-
27 shaped or reverse L-shaped (』).

1 26. The method as claimed in claim 25, wherein the
2 protecting layer is boro-silicate-glass (BSG).

1 27. The method as claimed in claim 25, wherein the
2 method for depositing the second spacers is LPCVD.

1 28. The method as claimed in claim 25, wherein the
2 second spacer is silicon dioxide.

1 29. The method as claimed in claim 14, wherein
2 forming a plurality of parallel shallow trench isolation
3 (STI) regions along a second direction, defining a
4 plurality of cell trenches, further comprises the steps
5 of:

6 sequentially performing photolithography and
7 etching, defining a plurality of parallel long
8 isolation trenches along a second direction,
9 stopping at the conductive layer therein; and
10 forming an third insulating layer in each long
11 isolation trench.

1 30. The method as claimed in claim 29, wherein the
2 third insulating layer is silicon dioxide.

1 31. The method as claimed in claim 29, wherein the
2 method of forming the third insulating layer is low
3 pressure chemical vapor deposition (LPCVD).

1 32. The method as claimed in claim 14, wherein
2 forming a drain region in the substrate adjacent to each
3 of the cell trenches further comprises the steps of:

4 removing the mask layer and the pad oxide layer,
5 exposing a plurality of active areas on the
6 substrate;
7 performing a drain implantation on the active areas;

8 performing a thermal annealing process, forming a
9 drain region in the substrate adjacent each
10 cell trench; and
11 forming a fourth insulating layer on each drain
12 region.

1 33. The method as claimed in claim 32, wherein
2 impurities used in the drain region implantation are N-
3 type impurities.

1 34. The method as claimed in claim 33, wherein the
2 N-type impurities comprise arsenic (As) ions.

1 35. The method as claimed in claim 32, wherein the
2 thermal annealing process is rapid thermal annealing
3 (RTA) process.

1 36. The method as claimed in claim 32, wherein the
2 fourth insulating layer is a silicon dioxide layer.

1 37. The method as claimed in claim 32, the method
2 for forming the fourth insulating layer is high density
3 plasma chemical vapor deposition (HDP CVD).